REMARKS

Applicants thank the Examiner for the courtesy of a personal interview on October 11, 2005.

The Final Office Action mailed May 13, 2005 and the Advisory Action mailed October 3, 2005 have been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

A "Petition for Extension of Time" for extending the due date for responding to the Office Action by two months and a check to cover the fee payment ($450.00) for the extension are filed with this Amendment. Authorization is granted to charge counsel's Deposit Account No. 01-2300, referencing **Attorney Docket No. 108066-00030**, for any additional fees necessary for entry of this Amendment.

Claims 1, 6, 11 and 17 have been amended. Applicants submit that the amendments made herein are fully supported in the Specification and the drawings, as originally filed, and therefore no new matter has been introduced. Accordingly, claims 1-17 are pending in the present application and are respectfully submitted for reconsideration.

The Advisory Action dated October 3, 2005 indicated that claim 11 was indefinite under 35 U.S.C. § 112, second paragraph. In the interview, the Examiner indicated that claims 1, 6, 11 and 17 may not be clearly described in the specification and that these claims may be unclear under 35 U.S.C. § 112. As discussed in the interview, Applicants have amended claims 1, 6, 11 and 17 so that these claims clearly recite the Applicants' invention.

Claims 1-3, 5-8, 10-13 and 15-17 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over the Yishay et al. patent (U.S. Patent No. 5,704,039) in view of the Akiyama et al. patent (U.S. Patent No. 5,784,464). Dependent claims 2-3 and 5, dependent claims 7-8 and 10, and dependent claims 12-13 and 15-16 depend from independent claims 1, 6 and 11, respectively. Claims 1, 6, 11 and 17 have been amended. The rejections are respectfully traversed and reconsideration is requested.

Independent claims 1 and 6, as amended, recite in part:

> ...an authentication circuit which is provided between the debug I/F circuit and a debug terminal for connecting outside, and for transmitting a transmission key from the debug terminal to outside, and authenticating from a reception signal received from the debug terminal and the transmission key to enable operation of the debug I/F circuit,
>
> wherein said internal circuit comprises a CPU connected to the debug I/F circuit through a debug bus and a peripheral circuit connected to the CPU through an internal bus separated from said debug bus, wherein said CPU writes said transmission key to said authentication circuit to start transmission of the transmission key.

Independent claim 11, as amended, recites in part:

> ...authenticating a reception signal received externally and the transmission key to enable operation of the debug I/F circuit,
>
> wherein the step of authenticating further comprises connecting a CPU to said debug I/F circuit through a debug bus and connecting a peripheral circuit to said CPU through an internal bus separated from said debug bus, wherein the step of authenticating further comprises a step of starting said transmitting step by writing said transmission key to said authentication circuit with said CPU.

Independent claim 17, as amended, recites in part:

> ...a discrimination device which is provided between said debug unit and said debug I/F circuit, and for receiving a transmission key from said authentication circuit, encrypting said transmission key by a predetermined key, and transmitting the

encrypted transmission key to said authentication circuit to enable debugging of said IC by said debug unit,

wherein said internal circuit comprises a CPU connected to said debug I/F circuit through a debug bus and a peripheral circuit connected to said CPU through an internal bus separated from said debug bus, wherein said CPU writes said transmission key to said authentication circuit to start transmission of the transmission key.

As discussed in detail in the interview on October 11, 2005, neither Yishay et al. nor Akiyama et al., either alone or in alleged combination, disclose or suggest the IC, the electronic device mounted with an IC, the debugging method and the debugger for debugging an IC, as recited in the present claims.

The Office Action took the position that Yishay et al., with reference to Fig. 1, discloses a circuit that includes a CPU 12 connected to a debug interface circuit (security buffer 13) through a debug bus and a peripheral circuit 14, 16, 18, 20 connected to the CPU through an internal bus (bus 36) separated from the debug bus. The system integration circuit 16 includes a security circuit 42 (shown in detail in Fig. 3).

This security circuit 42 in response to control signals 58, address signals 54 and data signals 56 activates or deactivates the secure mode for data processing system 10. As shown in Figs. 1-3 and disclosed in Yishay et al., security circuit 42 is connected to security buffers 13, 15, 17, 19, 21 and 24. This connection enables the security circuit to enable and disable the security buffers.

As discussed in detail in the personal interview, the security circuit 42 of Yishay et al., however, does not have any connection to terminals 24 that would allow the security circuit 42 to transmit a transmission key from terminals 24. Similarly, the CPU 12 does not write a key to security circuit 42.

Akiyama et al. is not cited for nor does it correct the above deficiencies in Yishay et al. Furthermore, Akiyama et al. appears to merely disclose a client-server based authentication system in which keys are generated, encrypted and exchanged to verify the identity of a client seeking access to services. Such does not disclose or suggest the IC, the electronic device, the debug method and the debugger of the present invention. Indeed, it does not appear that debug methods, debug I/F circuits and the like are mentioned anywhere in Akiyama et al. Accordingly, the combination of Yishay et al. and Akiyama et al. fail to disclose and/or suggest the claimed invention.

It is therefore submitted that the references, either alone or in alleged combination, fail to disclose or suggest the present invention as claimed. Based upon the foregoing, it is respectfully submitted that independent claims 1, 6, 11 and 17 are patentable and in condition for allowance. Reconsideration is respectfully requested.

It is further submitted that dependent claims 2-3 and 5, dependent claims 7-8 and 10, and dependent claims 12-13 and 15-16 are also patentable and in condition for allowance due to their dependency upon independent claims 1, 6 and 11, respectively, since the dependent claims differ in scope from the corresponding parent claims. Dependent claims 2-3 and 5 depend from independent claim 1, dependent claims 7-8 and 10 depend from independent claim 6 and dependent claims 12-13 and 15-16 depend from independent claim 11, and thus are further limited to additional features of the invention. Therefore, it is respectfully submitted that the dependent claims are patentable over the alleged combination of Yishay et al. and Akiyama et al. for at least the reasons set forth above with respect to independent claims 1, 6, 11 and 17.

Dependent claims 4, 9 and 14 were finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Yishay et al. in view of Akiyama et al. and further in view of Matsumura et al. (U.S. Patent No. 4,908,038). Dependent claims 4, 9 and 14 depend from independent claims 1, 6 and 11, respectively. The rejections are respectfully traversed and reconsideration is requested.

With reference to the above arguments concerning the independent claims, it is further submitted that Yishay et al., Akiyama et al. and Matsumura et al., either each alone or in the alleged combination suggested by the Office Action, do not disclose or suggest the invention recited in dependent claims 4, 9 and 14. While Matsumura et al. appears to disclose an IC card security feature in which output of processing result is waited by a timer in order to make a processing time constant from receipt of the processing request to output of the processing result, this reference is not cited for nor does it correct the deficiencies discussed above in Yishay et al.

Moreover, there is no suggestion to combine the references, as suggested by the Examiner in the Office Action. Specifically, none of the cited references are directed to preventing the exploitation of a debug I/F circuit when debug mode is enabled. Nor even if the references were combinable, as suggested, would such alleged combination result in the claimed invention since all of the references lack this claimed feature. It is therefore submitted that the dependent claims are also patentable and in condition for allowance. Reconsideration is requested.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned counsel at the telephone number, indicated below.

The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Deposit Account No. 01-2300, making reference to Docket No. 108066-00030.

Respectfully submitted,

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